

Remarks/Arguments

In the Office Action mailed on 16 May 2006, the Examiner rejected claims 1-23 under 35 U.S.C. §102(b) as anticipated by Shinozaki (United States Patent Number 6,333,875), and rejected claims 1, 2 and 18 under 35 U.S.C. §112 second paragraph as being indefinite. The Examiner objected to claim 18 as missing a period at the end of the claim. The Examiner objected to the specification as including an embedded hyperlink.

Applicants respectfully traverse the rejections and request reconsideration and withdrawal of the outstanding objections and rejections. Claims 1, 8, 13, 18 and 19 have been amended for editorial clarity and to better protect the invention. Claims 7 and 23 have been cancelled.

Objection to Claim 18

The Examiner objected to claim 18 as missing a period at the end of the claim. Applicants have amended claim 18 to correct this deficiency. In view of the amendment, Applicants respectfully request reconsideration and withdrawal of the objection to claim 18.

Objection to the Specification

The Examiner objected to the specification due to the presence of a hyperlink and required deletion thereof. Although incorporation by reference through a hyperlink is invalid, mere reference to a hyperlink as in the subject application as background information evidencing that which is readily known to those of ordinary skill in the art is permitted. The MPEP states that the Patent Office will render such links "inactive" for purposes of online publication. MPEP §608.1 states that:

Where the hyperlinks and/or other forms of browser-executable codes themselves rather than the contents of the site to which the hyperlinks are directed are part of applicant's invention and it is necessary to have them included in the patent application in order to comply with the requirements of 35 U.S.C. 112, first paragraph, and applicant does not intend to have these hyperlinks be active links,

examiners should not object to these hyperlinks. The Office will disable these hyperlinks when preparing the text to be loaded onto the USPTO web database.

The noted hyperlink of the specification is not intended as an improper attempt to incorporate by reference but rather is intended to merely point a reader to helpful background information evidencing that which is known in the art. Thus the hyperlink to background information enables the invention as required under 35 U.S.C. §112. In hopes of advancing prosecution of this application, Applicants have amended the specification to remove the "http://" prefix of the hyperlink to thus aid in rendering the embedded hyperlink references inactive for purposes of browsing online. Further, Applicants have removed now obsolete detailed portions of the URL since the Micron Corporation changed the location of the previously cited information. The URL as it remains merely points to reader to a typical source of background material where information regarding master delay circuits may be found. Applicants further hereby request that the Patent Office render the hyperlink inactive in any online publications thereof.

In view of the above discussion and the amendments to the specification, Applicants respectfully request reconsideration and withdrawal of the objection to the specification.

§112 Rejection

The Examiner rejected claims 1-2 and 18 under 35 U.S.C. §112, second paragraph, as being indefinite. Particularly, in regards to claims 1 and 18, the Examiner stated that the use of the relative term "substantially inherent" renders the claim indefinite. Applicants have amended claims 1 and 18 to replace "substantially inherent" with "substantially identical". Those of ordinary skill in the art would recognize the requisite degree of the term "substantially identical" as nearly identical, and differing by tolerances of the circuit using the delay components, of the intended speed and timing of the device, and of the fabrication processes used to fabricate the device.

In regard to claim 2, the Examiner stated that the term "substantially aligned" renders the claim indefinite. Those of ordinary skill in the art would recognize the

requisite degree of the term "substantially aligned" as nearly aligned, and differing by tolerances of the electronic circuit, the speed and timing of the circuit, and the fabrication processes generating the circuits. In a typical electronic circuit, two signals may not be identically aligned. However, tolerances of the circuit allow for two signals to be substantially aligned, and thus differ by design tolerances of the circuit. Thus, Applicants submit that the use of the relative terms "substantial" in the claims does not render the claims indefinite.

In view of the above discussion and the amendments to claims 1 and 18, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-2 and 18 under 35 U.S.C. §112.

35 U.S.C. §102(b) Rejection

The Examiner rejected claims 1-23 under 35 U.S.C. §102(b) as anticipated by Shinozaki.

The present application is related to systems and methods for latching data. Present day circuits have overhead delays caused by fabrication process variations and operating conditions of the circuit. These overhead delays may vary across the surface of the circuit, leading to varying delays at different physical locations of the integrated circuit die. Thus, a delayed signal generated at one physical location of the circuit with a particular designed delay value may be delayed due to local overhead variations in comparison with similarly delayed signals generated elsewhere on the circuit designed with the same delay value. Therefore, a data signal and a strobe signal may not be properly aligned, and data corruption may occur. The system of amended claim 1 solves this problem by providing a first delay circuit coupled to a strobe signal and a second delay circuit coupled to an associated data signal. The two delay circuits are in close physical proximity on the integrated circuit die. The first delay circuit programmably delays the strobe signal with a first delay to latch the data signal. Further, the first delay circuit has an overhead delay (e.g., an inherent delay other than the intended, designed

delay) that may vary based on fabrication process variations and/or operating conditions of the first delay circuit. The second delay circuit delays the data signal with a second delay that is substantially identical to the overhead delay of the first delay circuit. The substantially identical value of the first delay and the second delay is due to the inherent overhead in both delays due to their close physical proximity and similar fabrication variations and operation conditions. Thus, the first delay and second delay allow the data signal and strobe signal to align more closely.

By contrast, Shinozaki discloses a semiconductor circuit which receives a strobe signal and a data signal. The circuit includes a latch-signal-generation circuit which generates a first latch signal delay by a first delay time relative to the strobe signal and a second latch signal inverted and delayed by a second delay time relative to the strobe signal. A control circuit adaptively controls the latch signal-generation circuit to adjust timings of the first and second latch signals such that the first delay time and the second delay time become substantially equal. The data signal is then latched at edge timings of the first and second latch signals. Thus, the strobe signals are created with delays substantially equal for latching a data signal at rising and falling edges of a clock signal (see Abstract of Shinozaki).

Shinozaki does not disclose nor reasonably suggest two delay circuits in close proximity for generating delays of the strobe signal and data signal with substantially identical overhead delays. Rather, Shinozaki discloses creating adjustable delays *ta* and *tb* such that the difference between the two delays is substantially zero (e.g., within a specific tolerance) (Shinosaki, col 4, lines 8-21). Thus, multiple latch signals may be aligned with rising and falling edges of the strobe signal.

Amended claim 1 of the present application recites that the first delay circuit has an overhead delay that may vary based on fabrication process variations or operating conditions or both fabrication process variations and operating conditions of the first delay circuit. This overhead delay may be localized, and may cause data signals and strobe signals to be mis-aligned and out of synchronization. Shinozaki does not disclose delays in a delay circuit having "overhead delays" as defined by amended claim 1.

Further, Shinozaki does not disclose delaying the data signal with a second delay circuit having an overhead delay that is substantially identical to the overhead delay of the first delay circuit. While Shinozaki does show a delay circuit on the data signal pathway (28), the delay circuit is not shown to have an overhead delay identical to an overhead delay of another delay circuit associated with the strobe signal. Further, the delay generated by the delay circuit in the data signal pathway of Shinozaki does not appear to be dependent on delays in other functional elements of the circuit (e.g., the latch signal pathway). Shinozaki discloses creating a dummy-variable circuit for emulating delays of rising edges of the input data signal (col 13, lines 1-5). The comparison circuit 160 of Shinozaki then can adjust a delay of the variable-delay circuit 155 on the data input signal pathway. However, the adjustable delay is based on emulation of an identically configured signal pathway and not on overhead delays of other signal pathways carrying different signals. Thus, Shinozaki discloses a different approach for creating delays on the data signal pathway.

In regard to claim 7 (now cancelled), the Examiner stated that Shinozaki discloses "the first and the second delay circuits comprise substantially the same integrated circuit such that the first delay circuit comprise a first overhead substantially having the second delay and the second delay circuit comprises a second overhead having the second delay" (cited as Shinozaki, col 6, lines 30-43). The essential elements of claim 7 have been incorporated into claim 1. However, Shinozaki does not disclose the elements of claim 7. Shinozaki discloses that the dummy circuit has the same configuration as the input circuit (col 6, lines 30-32), and that another dummy circuit has the same configuration as the delay circuit (col 6, lines 37-39). However, these circuits are not equivalent to the first and second delay circuits of the presently claimed system. Specifically, the dummy circuits do not apply a delay to active signals of the circuit. Rather the dummy circuits emulate delays to allow the comparison circuit to adjust the delays of the delay circuit and the input circuit. Additionally, Shinozaki does not disclose circuits comprising overhead delays, nor does Shinozaki disclose differing delay circuits having equal overhead delays. Thus, Shinozaki does not disclose the elements of claim 7. These same arguments apply to claim 23, now cancelled and incorporated into independent claim 18.

In view of the above discussion, Applicants maintain that amended independent claim 1 is distinguished over the teachings of Shinozaki. The claims are neither taught nor reasonably suggested by the teachings of Shinozaki considered alone or by any art of record, considered individually or in any combination. Applicants maintain that independent claims 8, 13 and 18 are distinguished for at least the same reasons discussed above.

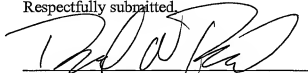
Dependent claims 2-6, 9-12, 14-17 and 19-22 are allowable for at least the same reasons and as dependent upon allowable base claims 1, 8, 13 and 18 respectively. Applicants respectfully request reconsideration and withdrawal of the outstanding rejections of claims 1-6 and 8-22.

Conclusion

Applicants have amended independent claims 1, 8, 13 and 18 and dependent claim 19 for editorial clarity and to better protect the invention. Applicants have amended claims 1 and 18 to overcome the Examiner's §112 rejections thereof and the Examiner's objection to claim 18. Applicants have amended the specification to overcome the Examiner's objection thereto and have Applicants have cancelled claims 7 and 23. The Examiner's rejection of all claims 1-23 has been thoroughly discussed. Applicants have requested reconsideration and withdrawal of all outstanding objections and rejections.

Applicants have submitted herewith a petition for a one month extension of time to reply along with appropriate fees for the petition. Otherwise, Applicants believe that no other fees are due in this matter. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,



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